A Method to Overcome Self-Heating Effects in SOI MOSFETs

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Abstract: Self heating of a MOS device will reduce performance. Drain current decreases and long term reliability can be affected. In SOI devices, self-heating is an even greater problem due to the buried oxide. By adding a path from SOI to substrate that has a high thermal conductivity and low electrical conductivity, the negative effects of self-heating can be reduced.

Key words: SOI, MOSFET, self-heating effect
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0 Introduction

Self heating has negative effects in most devices. In silicon-on-insulator (SOI) MOSFETs, where a device is often completed surrounded by oxide, the negative effects are compounded. It will increase the lattice temperature and degrade mobility leading to reduced drain current. This paper will discuss three types of heat sinks to allow impact ionization generated heat to be dissipated.

1 Self Heating

Self heating is very important to the operation of SOI devices, especially those with thin Si films. In a bulk device, heat is quickly spread throughout the silicon and has little effect. In a standard SOI device, the silicon film is surrounded by silicon dioxide, which acts as a trap for the heat. SiO_2 has a thermal conductivity (K) of 1.5 W/m·K, while the conductivity of silicon is 98.9W/m·K. Since K_{Si} is greater than K_{SiO_2}, silicon will conduct heat much easier than silicon dioxide. Fig. 1, a measurement of a 0.16 μm gate length, 5 μm width, a 100 nm buried oxide (BOX), and a 120 nm silicon film (T_{Si}), demonstrates the effects. With a gate voltage (V_g) of 1.5V, the drain current (I_d) actually decreases with increasing drain voltage (V_d). This phenomenon is a direct result of self heating reducing mobility thereby degrading drain current. Self heating can also jeopardize long term reliability[1].

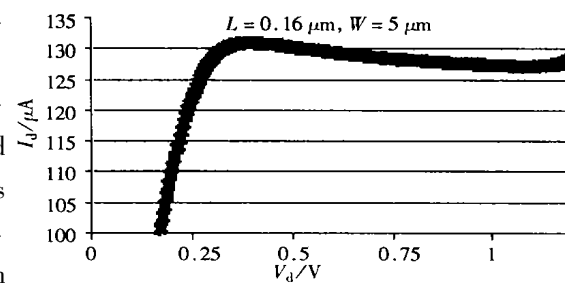

Fig. 1 Demonstrates decreasing drain current with increasing drain potential due to self heating

2 Heat Sink Design and Process

The key idea is to design a method to allow heat conduction from the silicon film to the bulk while keeping the

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film electrically isolated so that the advantages of SOI devices are still achieved. A method to reduce heat accumulation in SOI devices was developed by Wensong, *et al*. They start with a standard wafer, grow SiO_2 for the BOX, then deposit a layer of polysilicon for the source/drain region. An etch step removes polysilicon and SiO_2 from the channel, where an epitaxial layer is grown for the channel. This is a complex process.

Several simpler processes are now proposed that use SIMOX wafers and do not require the growth of an epi layer. One such method is to etch a high aspect ratio hole through part of the shallow trench isolation (STI) oxide and fill the area with a heat conducting material. This can be implemented on both the source and drain sides, or source side only. Fig. 2(a) demonstrates the source and drain heat sink. The polysilicon heat sink makes direct contact to the source and drain through the total thickness of the silicon film.

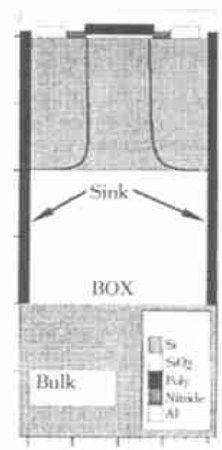

Fig. 2(a) cross section a source drain heat sink

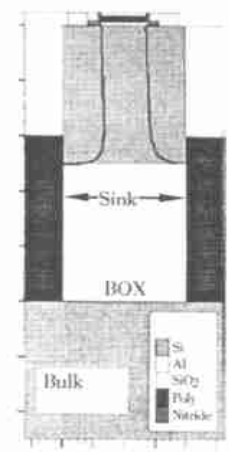

Fig. 2(b) cross section of a STI heat sink

STI sink, a third method, involves placing the sink directly underneath the STI. After shallow trench isolation etch, an oxide etch would be needed to create a hole in the BOX. With an additional lithography level, the sink could be masked to create a gap between adjacent sinks, allow for isolation. Polysilicon, or some other heat conducting material, would then be deposited into the hole at a thickness that is greater than the BOX thickness, creating overlap between the source/drain and sink for heat conduction. Poly deposition is followed by STI oxide growth and deposition. See Fig. 2(b). In all three heat sinks, later rapid thermal anneals drive dopants into the sink, creating some electrical conduction. Although other materials could be used, all simulation in this paper assume polysilicon sinks.

3 Heat Sink Results

With a source and drain sink, simulations show a large increase in saturation drain current. Fig. 3 is a plot of simulated drain current for each type of sink, using a $V_g = 1.5$ V, $T_{Si} = 100$ nm, BOX = 100 nm, and gate length = 0.13 μm. For example, at $V_g = V_d = 1.5$ V, a 30.4% increase in current between a 20 nm wide heat sinked device and a control device was realized. A two sided 10 nm wide sink gave a 24% increase in drain current. A heat sink on both the source and drain sides leads to good thermal efficiency but also increased device size and leakage to the bulk (due to the high reverse bias on the drain). With source side sink only, and $V_g = V_d = 1.5$ V, a 9.6% increase in drain current is realized with a 10 nm wide heat sink, and 18% increase is achieved with a 100 nm sink. The current increase is not as large as the double sided sink, but still show a significant improvement. The STI sink allowed 686 μA/μm of drain current, or a 24.7% increase. The STI simulations were done with 10 nm of overlap between the substrate and sink. This could be adjusted to allow more heat transfer or more isolation. Sink results are summarized in table 1.

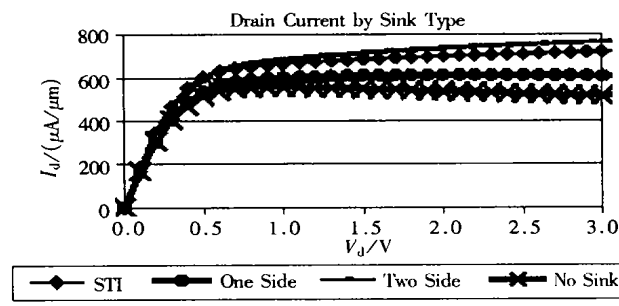

Fig. 3 Drain current comparison of sink types

The single-sided sink showed a 34.2% reduction of temperature at V_d= 3.1 V, while the double sided 10 nm and 20 nm heat sink showed a 33.7% and 38.7% reduction respectively. The best method to reduce heat build up was the STI heat sink, which resulted in a temperature reduction of 44.2%. Lattice temperatures are demonstrated in Fig. 4.

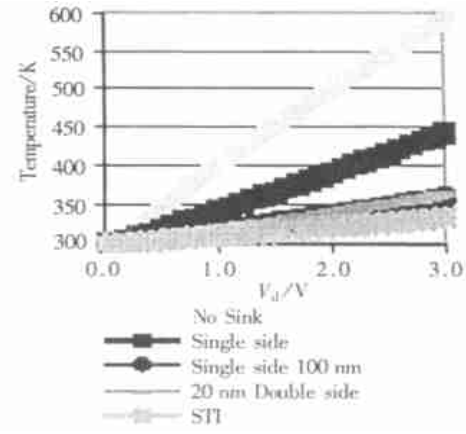

Fig. 4 Lattice temperature with and without sinks

A critical measurement for a heat sink of this design is leakage through the sink to the bulk. Although a PN junction forms when the sink and bulk meet, some low level leakage can still occur. This test is performed by setting V_g and source potential (V_s) to ground, and V_d = 1.5 V. Current leakage on a two sided device was approximately 75 μA/μm. Applying a -1V back bias on the bulk decreased leakage by three orders of magnitude. The optimum leakage of < 1 nA/μm is obtained by building a sink on the source side only or under the STI.

Table 1 Heat sink results

Size and type of sink	Drain current (μA/μm)	Increase in Real Estate	Percent Drain Current Improvement	Lattice Temperature/K
Control	550	0%	0%	452
10 nm 2 side	682	5%	24.0%	341
20 nm 2 side	717	10%	30.4%	329
10 nm 1 side	611	2.5%	11.1%	366
100 nm 1 side	650	25%	18.2%	328
STI	686	0%	24.7%	316

4 Conclusion

Self heating generally has undesired effects on devices. Because of the isolation of SOI devices, they are particularly vulnerable to self heating caused MOSFET operation in saturation. Adding a heat sink to the device can greatly reduce the effects of self heating. Various positions and sizes were modeled. The smaller size sinks on the source side were optimal for minimizing leakage, while large, drain and source sided sinks were best for maximizing drain current (including bulk and drive). STI sinks were best for maximizing drive (from source to drain) current and minimizing drain to source leakage.

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一种克服 SOI MOSFET 器件自加热效应的方法

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[摘要] MOS 器件的自加热效应将影响器件的性能. 漏极电流将减小, 长时间的可靠性也会受到影响. 在 SOI 器件中, 自加热甚至比埋葬式氧化物引起的问题更严重. 本文通过在 SOI 和基片之间增加一条具有高导热和低导电的路径, 减小了自加热的负面效应.

[关键词] SOI 硅一绝缘体, MOSFET 器件, 自加热效应

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The Determination of the Dissociation Constants of α-Naphthol and β-Naphthol in Ethanol/Water Mixed Solvent by Potentiometric Titration

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Abstract: The dissociation constants of phenol, α-naphthol and β-naphthol in water-ethanol mixed solvent (I = 0.10 mol/L, KCl) were determinded by potentiometric titration. The results showed that the pK_a was a good linear function of the volume fraction of ethanol in the concentration range studied. The dissociation constants of phenol, α-naphthol and β-naphthol in water were determinded by extrapolation to be 9.80, 9.40 and 9.67 under the conditions of this experiment.

Key words: phenol, α-naphthol, β-naphthol, mixed solvent, dissociation constants, potentiometric titration

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