Optimizing Dynamic-Threshold DTMOS Device Performance in an SOI Embedded DRAM Technology

Kim C S[1], Burke F[1], Rambhatla A[1], Zhao Y[1,3], Zahurak J[2], Parke S A[1]

(1. Department of Electrical & Computer Engineering, Boise State University, 83725, Idaho, USA)
(2. Micron Technology Inc, 83707, Idaho, USA)
(3. College of Electrical and Electronic Engineering, Nanjing Normal University, 210042, Nanjing, PRC)

Abstract: This paper describes the DC and high frequency characteristics of a dynamic threshold DTMOS *n*-channel device, fabricated within a low-cost CMOS SOC process which also includes high-density embedded DRAM. The DTMOS device design in this process was previously found to be superior to both grounded body (GB) and floating body (FB) MOSFETs. This DTMOS device achieves kink-free behavior, with g_m = 936 μS/μm, g_{out} = 36 μS/μm, I_{on}/I_{off} = 210 μA/0.1 pA, S = 67 mV/dec, and f_{max} = 32 GHz at V_{DD} = 1 V. These DTMOS devices are excellent for sub-volt embedded baseband circuits with sufficient performance for RF front-end circuits, thus enabling the combination of embedded DRAM, digital, analog, and RF circuit cores in, ultra-low-power, low-cost SOCs.

Key words: dynamic-threshold DTMOS device, SOI, embedded DRAM technology
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0 Introduction

By scaling MOSFET channel lengths to the 100 nm regime, CMOS is rapidly becoming a serious option for many low-power, wireless RF applications that were previously considered to be the exclusive domain of more expensive SiGe BiCMOS and GaAs technologies. However, there are severe limitations to achieving digital, analog, and especially RF and DRAM integration on a single CMOS SOC. Fortunately, SOI offers solutions to several of these integration problems, including reduced power dissipation and capacitances, reduced substrate coupling and losses, simplified well processing, reduced latchup, reduced SER, and improved DRAM retention. However, floating-body PDSOI devices must contend with non-linearity, excess $1/f$ noise, and reduced output resistance, due to the parasitic bipolar action in the body. The Dynamic Threshold (DTMOS) mode of device operation, where the floating body/well is tied to the gate, has recently been investigated as an ideal SOI device implementation for sub-volt analog and RF circuits[1~7].

1 Process/Device Description

The devices used in this work were processed in a low-cost 0.15 μm bulk CMOS DRAM process that was mapped onto low-dose SIMOX substrates (Table 1). This process utilizes nitrided 4 nm gate oxide and WSix poly gates, without silicided source/drains. Shallow S/D extensions, retrograde body, and halo implants were used to improve short-channel behavior and reduce parasitic BJT action. A

Table 1 Process and Device Parameters

SIMOX, T_{soi} = 150 nm, T_{box} = 200 nm
T_{ox} = 40 nm
L_{min} = 0.15 μm

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Biography: Kim C S, Korean, born in 1968, postdoctoral in department of Electrical & Computer Engineering, Boise State University; his research interest includes IC design, device modeling and characterization.

new compact "H-gate" DTMOS transistor layout was used to minimize area and parasitic capacitance (Fig. 1).

2 Results & Discussion

Table 2 summarizes the NMOS and PMOS device results for GB, FB, and DT modes of device operation at V_{DD} = 1 V. In most categories, the DT mode shows substantial advantages, particularly in transconductance and current drive. The GB device shows lowest performance, with the FB device in between. Figs. 2~ 3 show the input characteristics. At one volt, the DTNMOS draws an input current of 1 μA/μm, with a drive current of 206 μA/μm, a transconductance of 936 μS/μm, and an output conductance of only 36 μS/μm. The same device has an I_{off} = 0.13 pA/μm, due to 0.20 V of dynamic V_t shift. The PMOS device has a lower V_t, but exhibits 0.30 V of dynamic V_t shift. Figs. 4~ 5 show the output characteristics. The DTNMOS does not exhibit the kink and degraded g_{out} like the floating body device. Fig. 6 shows I_{on} vs. I_{off} for the DTNMOS. These are excellent analog properties, in addition to much lower $1/f$ noise for DTMOS devices published recently[6]. Microwave test structures were fabricated and tested using a Cascade/HP8510C VNA S-parameter system. Fig. 7 shows the maximum power gain vs. L_{eff} for the DTMOS devices. Figs. 8~ 9 show the device power and current gain vs. frequency. These results demonstrate the capablity of this technology to support embedded RF circuits. F_{max} is 32 GHz for DTNMOS and 20 GHz for DTPMOS at V_{DD} = 1 V. By scaling L_{eff} of the DTMOS device to 50 nm, F_{max} > 100 GHz should be achieveable.

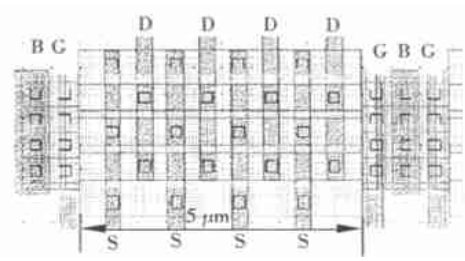

Fig. 1 Layout of the compact "H-gate" interdigitated DTMOS transistor, with four 5 μm gate fingers and gatete-body metal connections at both sides of the device. This W = 20 μm block is replicated 8 times to build a W = 160 μm RF transistor.

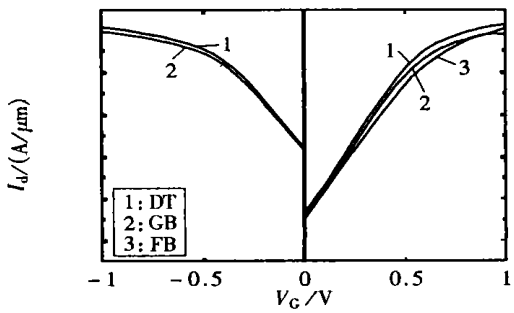

Fig. 2 CMOS subthreshold characteristics at V_D = 1 V, showing nearly ideal S for DT and a high V_t for the DRAM NMOS.

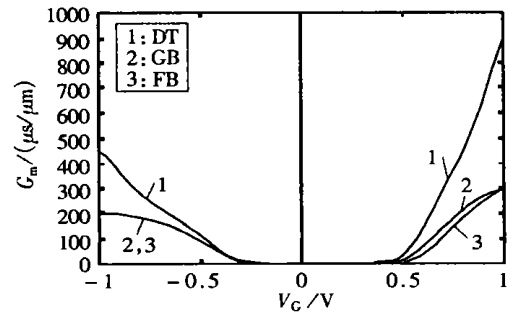

Fig. 3 CMOS transconductance at V_D = 1 V, showing a 3X improvement for DTNMOS and 2X for DTPMOS.

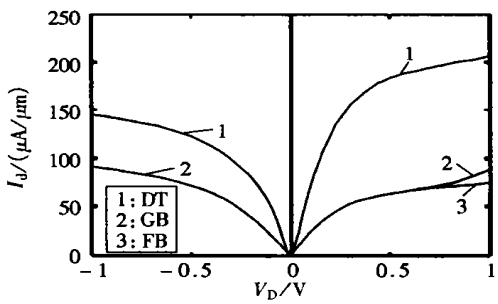

Fig. 4 CMOS drive current at V_G = 1 V, showing a 2.5X improvement for DTNMOS and 1.5X for DTPMOS.

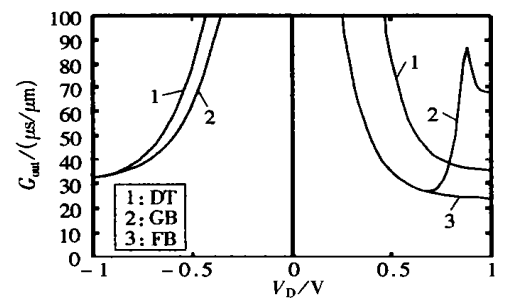

Fig. 5 CMOS output conductance at V_G = 1 V, showing similar results, except for the obvious FB kink.

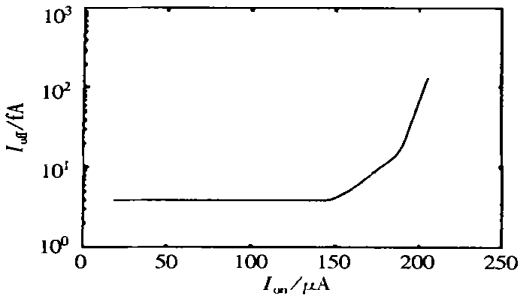

Fig. 6 I_{on} vs. I_{off} at V_D= 1 V showing that the DRAM DTNMOS has low I_{off} and low I_{on}.

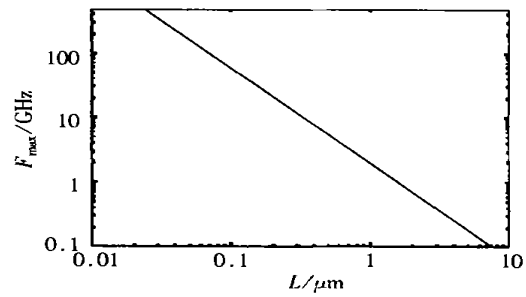

Fig. 7 Maximum power gain frequency vs. channel length for the DTNMOS, showing potential performance possible by scaling.

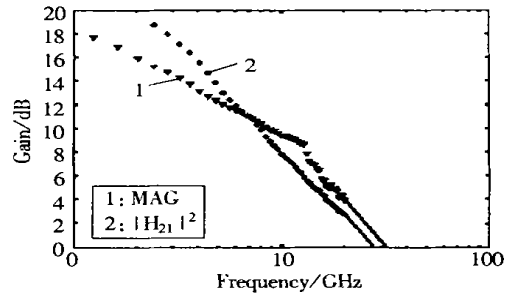

Fig. 8 Gain vs. frequency at V_G= V_D= 1 V, L= 0.15 μm, W= 160 μm for a DTNMOS RF transistor.

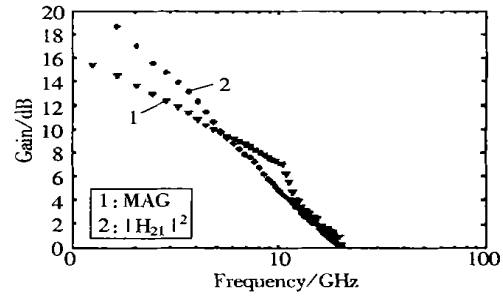

Fig. 9 Gain vs. frequency at V_G= V_D= −1 V, L= 0.15 μm, W= 160 μm for a DTPMOS RF transistor.

Table 2 Device Results

Parm	Units	Grounded Body		Floating Body		DTMOS	
		nmos	pmos	nmos	pmos	nmos	pmos
I_{on}	uA/um	75	92	87	93	206	145
I_{off}	pA/um	0.11	216	0.18	220	0.13	238
V_t	V	0.67	−0.45	0.66	−0.45	0.86	−0.75
S	mV/dc	75	87	75	87	67	86
G_m	uS/um	291	206	296	207	936	451
g_o	uS/um	24	33	68	33	36	32
F_{max}	GHz	22	15	25	17	32	20

3 Acknowledgment

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[References]

[1] Goldman D, Degregorio K, Kim C S, *et al*. 0.15μm SOI DRAM technology incorporating sub-volt dynamic threshold devices for embedded mixed-signal & RF circuits[A]. IEEE SOI Cnoference, 2001.97~98.

[2] Parke S A, Hu C, Ko P K. Bipolar-FET hybrid-mode operation of quarter-micrometer SOI MOSFET[J]. IEEE EDL, 1993, 14(5): 234~236.

[3] Assaderaghi F, Sinitsky D, Parke S, *et al*. A dynamic threshold Voltage MOSFET (DTMOS) for ultra-low voltage operation[A]. International Electron Devices Meeting, 1994. 809~812.

[4] Assaderaghi F, Sinitsky D, Parke S A, *et al*. Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI[J]. IEEE TED, 1997, 44(3): 414~422.

[5] Tanaka T, Momiyama Y, Sugii T. F_{max} enhancement of dynamic threshold-voltage MOSFET (DTMOS) under ultra-low supply volt-

age[A]. International Electron Devices Meeting, 1997.423~426.

[6] Ferlet-Cavrois V, Bracale A, Fel N, *et al*. High frequency characterization of SOI dynamic threshold voltage MOS (DTMOS) transistors[A]. IEEE SOI Conference, 1999.24~25.

[7] Momiyama Y, Hirose T, Kurata H, *et al*. A 140 GHz f_t and 60 GHz f_{max} DTMOS integrated with high-performance SOI logic technology[A]. International Electron Devices Meeting, 2003.451~454.

[8] Yagishita A, Saito T, Inumiya S, *et al*. Dynamic threshold voltage damascene metal gate MOSFET(DT-DMG-MOS) with low threshold voltage, high drive current, and uniform electrical characteristics[A]. International Electron Device Meeting, 2000.663~666.

SOI 嵌入式 DRAM 技术动态钳制电位 DTMOS 器件性能的优化设计

Kim C S[1], **Burke F**[1], **Rambhatla A**[1], 赵阳[1,3], **Zahurak J**[3], **Parke S A**[1]

(1. 美国爱达荷州 BOISE 州立大学电气与计算机系, 83725, 爱达荷州)

(2. 美国 Micron 公司, 83707, 爱达荷州)

(3. 南京师范大学电气与电子工程学院, 210042, 南京)

[摘要] 描述了 *n*-沟道动态电位 DTMOS 半导体器件的直流和高频特性, 该器件制造采用了低功耗 CMOS SOC 工艺, 同时也包含了高密度嵌入式 DRAM 技术. 在本工作中的 DTMOS 器件在较早时候就发现性能优于本体接地(GB)和本体浮地(FB)的 MOSFET 器件. 本器件具有无特性曲线缠绕、g_m = 936 μS/μm, g_{out} = 36 μS/μm, I_{on}/I_{off} = 210 μA/0.1 pA, 在 V_{dd} = 1 V 时 f_{max} = 32 GHz 的良好特性, 特别适用于低电压嵌入式基频电路并具有对射频 RF 前端电路的极佳性能, 因此可以使嵌入式 DRAM、数字电路、模拟电路和 RF 射频电路混合于一体, 用在超低功耗、低成本的 SOC(系统集成)芯片系统中.

[关键词] 动态钳制电位 DTMOS 器件, 系统集成芯片, 嵌入式 DRAM 技术

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