

Quest for the Ultimate Sub-50 nm CMOS Transistor Structure

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Abstract: In this paper, the work is introduced on investigation on non-classical CMOS structure in the quest to find the ultimate transistor structure that will permit evolutionary improvements of the existing CMOS technology base.

Key words: CMOS, non-classical CMOS structure, transistor structure

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1 Background & Motivation

Recently, much attention has been given to “beyond CMOS” technologies such as quantum dots, single electron transistors, carbon nanotube transistors, molecular transistors, and even biological transistors. However, significant technological improvements are still needed in what the 2001 ITRS Roadmap refers to as “Nonclassical CMOS transistor structures.” There are many recently studied or proposed structures in this category which are discussed in the 2001 Roadmap. In this work, we seek to comparatively investigate these structures from first-principles in the quest to find the ultimate transistor structure that will permit evolutionary improvements of the existing worldwide CMOS technology base, complementing the inevitable revolutionary CMOS replacement technologies.

Fig. 1 shows simple channel crosssections (normal to current flow) of various proposed gate structures. A) Ultra-Thin Body (UTB) or Fully-Depleted (FD-SOI), B) FinFET, C) Surround Gate or Vertical Pillar, D) Planar Independent Double-Gate, E) Triple-Gate and F) Quad-Gate. Note that no particular wafer plane is assumed in these diagrams, and that these six gate structures could theoretically be built in an X, Y, or Z configuration. This work does not seek to determine which structure is the most viable or cost effective to build, but instead which structure results in the most favorable electrical performance.

As MOSFETs are scaled below 50 nm channel lengths, there are many challenges: shortchannel effects, high-field effects, extrinsic parasitic effects, self-heating, voltage scalability, current drive, tunneling leakages, and manufacturability are some of the major ones. In the past, tighter lithography, higher doping, thinner gate dielectrics, thinner channels, thinner S/D junctions and complex vertical and lateral implants have been utilized. However, each of these tools are approaching fundamental physical limits which will make further scaling of conventional bulk and SOI device structures very difficult^[1]. Multiple-Gate MOSFET structures solve many of these issues, but the complexity of fabricating these is a big challenge. Fig. 2 shows a simple double damascene gate structure which has a superior

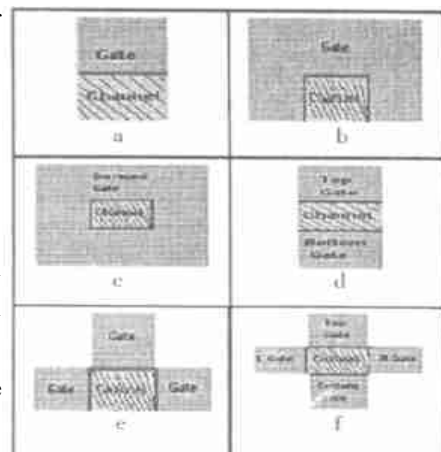


Fig. 1 Simple channel crosssections of various proposed gate structure

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performace compared to a single gated structure. This is shown in the summary table.

Table 1 Summary Table

| | Single Gate | Double Gate |
|--------------------------|-------------|-------------|
| I_{on} (mA/ μ m) | 0.65 | 1.26 |
| I_{off} (nA/ μ m) | 20 | 0.2 |
| V_{th} (V) | 0.35 | 0.39 |
| Sub- V_{th} (mV/dec) | 76 | 67 |
| g_{msat} (mS/ μ m) | 1.12 | 2.5 |
| DIBL | 0.15 | 0.07 |
| L_{eff} (nm) | 50 | 50 |
| T_{ox} (nm) | 2 | 2 |
| Channel Thickness(nm) | 16 | 16 |
| S/D Thickness(nm) | 68 | 120 |

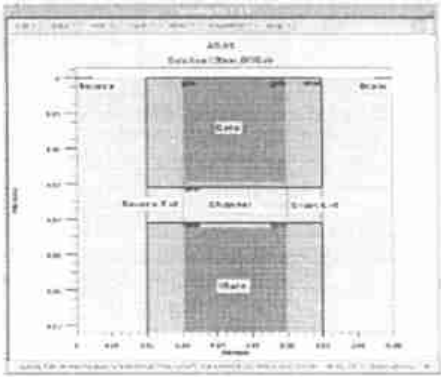


Fig. 2 A simple double damascene gate structure

In this paper, we will focus on comparing a couple of these proposed structures, namely, the planar, damascene single- and double-gated devices, since they are the most evolutionary from the current planar CMOS technology. In several respects, the double-gated MOSFET offers better characteristics than the single-gated MOSFET. When there are two or more gates surrounding the channel, the electric field of the drain is more effectively screened, enabling shorter channel designs. DG MOSFETs with midgap workfunction gates and no channel doping also have acceptable threshold voltages and very good mobility^[3]. They also have less V_t variation due to elimination of doping variations^[2]. However, the channel thickness must be aggressively thinned, leading to high resistance S/D's, unless some raised or Damascene S/D structure is employed.

Extensive DC device simulation of these structures has been accomplished using Silvaco's ATLAS simulator. These simulated structures do not include an assumed substrate structure and are therefore generic with regard to their X, Y, Z orientation. They could be built in either bulk or SOI processes, but SOI provides more flexibility. Although most of the simulations were accomplished by incorporating the drift-diffusion model, which cannot predict absolutely accurate results for very shortchannels, relative comparisons between these various device structures are still valid. The conventional drift-diffusion model for charge transport neglects non-local transport effects such as velocity overshoot, diffusion associated with carrier temperature and dependence of impact ionization rates on carrier energy distribution. Hence more advanced energy balance and hydrodynamic models are becoming necessary for simulating deep submicron devices. Devices with channel lengths 20~ 100 nm, channel thicknesses 5~ 25 nm, gate oxide thicknesses 0.5~ 2.5 nm, and S/D thicknesses 36~ 56 nm for the Single Damascene Gate (SDG) device and 67~ 87 nm for the Double Damascene Gate (DDG) device were simulated in this study. Midgap metal gates with a workfunction of 4.8 V (i.e. TiN) were utilized to enable totally undoped channels with appropriate threshold voltages.

Fig. 3 compares the V_{th} roll-off curves of a typical SDG and a DDG. SCE is adequately controlled for the DDG down to 20 nm lengths. The double-gated threshold voltage is clearly more scalable than the single-gated MOSFET. Tunable threshold voltages can be obtained by using variable-workfunction metal gates. This eliminates the painstaking process of doping the channel very precisely to obtain the desired V_{th} . Also, it improves the mobility of the carriers in the channel, due to no dopant scattering.

Fig. 5 shows the short channel subthreshold slope and DIBL behaviour for both SDG and DDG devices. The DDG device shows essentially no SCE down to 20 nm while the SDG device is limited to 50 nm or longer. Fig. 6 shows the drive current vs. L_{eff} , showing dramatically increased current drive of the DDG. The double gated device has about 2X higher current drive and transconductance and nearly ideal sub-threshold slope. In addition to DDG having two channels, its structure allows thicker source/drains for lower resistance than SDG. Hydrodynamic charge transport simulation was also applied to these short channel devices, resulting in a 40% further increase in drive

current over the drift/diffusion simulations.

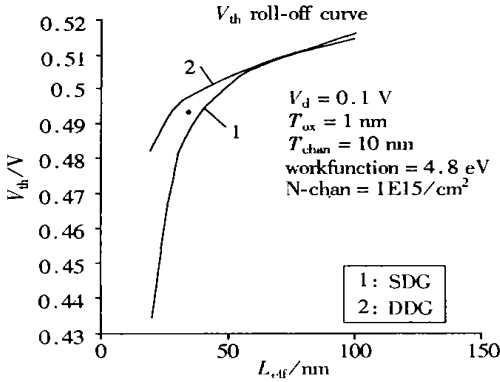


Fig. 3 Comparison of the V_{th} roll-off curves of a typical SDG and a DDG

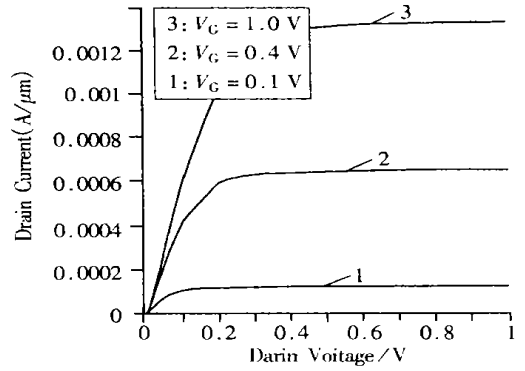


Fig. 4 I_D vs V_D curve of a DDG

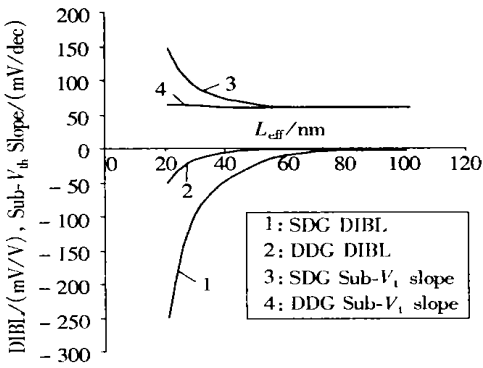


Fig. 5 Short-channel subthreshold slope and DIBL behavior for both SDG and DDG

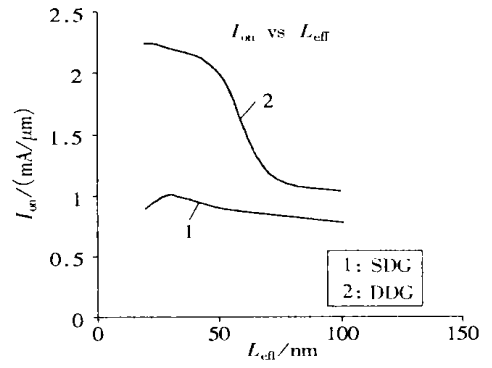


Fig. 6 Device current vs. L_{eff}

Fig. 7 shows the effect of gate oxide thickness variation on Sub- V_{th} slope and DIBL. Both Sub- V_{th} slope and DIBL improve with thinner T_{ox} . However, T_{ox} must be thinner than 1 nm for adequate SCE control in the SDG device, while the DDG device can use 2.5 nm T_{ox} . Fig. 8 shows the effect of gate oxide thickness variation on drive current. I_{on} increases with thinner T_{ox} more linearly for the DDG device than the SDG device. Fig. 9 shows the effect of channel variation on drive current. The drive current decreases with decrease of channel thickness as opposed to increasing, this is because of increase in the series resistance of the source/drain regions as they grow thinner. Fig. 10 shows the effect of channel thickness variation on the electrostatics of the device. Both DIBL and Sub- V_{th} slope are reduced as the channel thickness is reduced which implies improved SCE. The SDG device requires thicknesses less than 10 nm for adequate SCE control, while the DDG device can use channel thicknesses up to 25 nm.

2 Conclusion

It is clearly shown that a double gated device has superior short-channel characteristics and better current drive. At this point of our study we conclude that a double gated device is a structure that will permit evolutionary improvements of the existing worldwide CMOS technology base without having to look into revolutionary CMOS replacement technologies.

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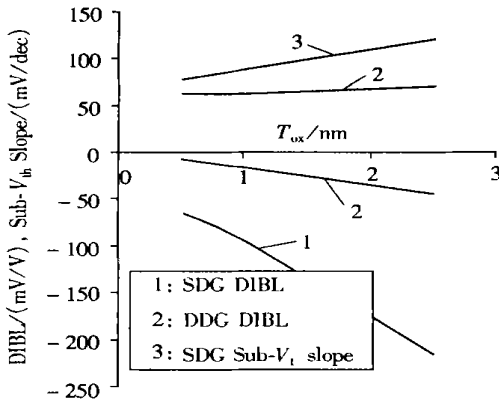


Fig. 7 Effect of gate oxide thickness variation on Sub- V_{th} slope and DIBL

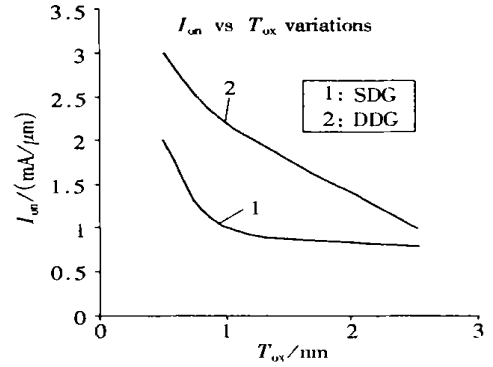


Fig. 8 Effect of gate oxide thickness variation on drive current

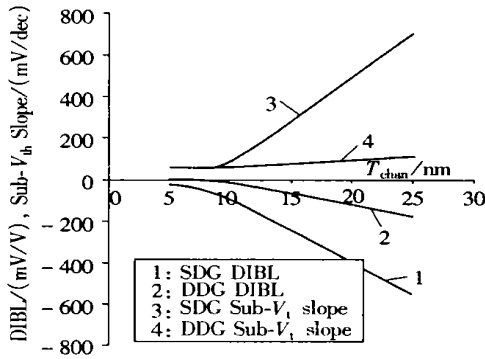


Fig. 9 Effect of channel variation on drive current

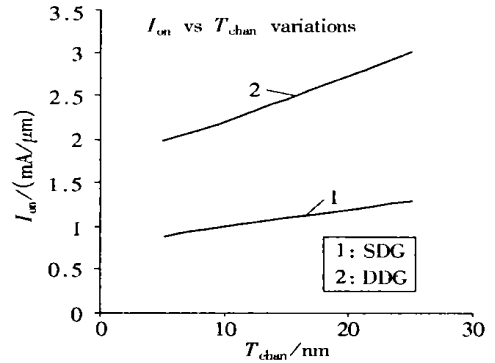


Fig. 10 effect of channel thickness variation on the electrostatic of device

[References]

- [1] Wong H S P. Design and performance considerations for sub-0.1 μm double-gate SOI MOSFETs[A]. International Electronic Device Meeting, 1994.
- [2] Wong H S P, Chan K K, Taur Y. Self-aligned double-gate MOSFET with a 25 nm thick channel[A]. International Electronic Device Meeting, 1997. 427~ 430.
- [3] Wong H S P, Frank D J, Solomon P M. Device design considerations for double-gate, ground plane, and single-gated ultra-thin SOI MOSFETs at the 25 nm channel length[A]. International Electronic Device Meeting, 1998. 407~ 410.

寻求最终亚-50 纳米 CMOS 器件结构

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[摘要] 主要介绍了对各种非典型 CMOS 结构的研究, 从而寻求最终的结构模式适应不断变化的 CMOS 发展技术。

[关键词] CMOS 器件, 非典型结构, 晶体管结构

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