

# Source/ Drain Optimization of the Dynamic-Threshold DTMOS Device in a 0.15 $\mu\text{m}$ SOI Embedded DRAM Technology

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**Abstract:** This paper describes experimental results used to optimize the source/ drain implant design of a dynamic threshold DTMOS  $n$ -channel device, fabricated within a low-cost 0.15  $\mu\text{m}$  SOI CMOS System-On-Chip process, which also included high-density embedded DRAM. A shallower, lower dose S/D implant was found to lower the body resistance and DIBL, thus increasing the dynamic body effect. The DTMOS device design in this process was previously found to be superior to both grounded body (GB) and floating body (FB) operation<sup>[1]</sup>, with  $I_{\text{on}} = 656 \mu\text{A}/\mu\text{m}$ ,  $I_{\text{off}} = 3 \text{ pA}/\mu\text{m}$ ,  $S = 64 \text{ mV}/\text{dec}$ , and  $G_m = 1.690 \mu\text{S}/\mu\text{m}$  at  $V_{\text{dd}} = 1.0 \text{ V}$ . This DTMOS device was also previously shown to have excellent analog and RF performance, with  $F_{\text{max}} = 32 \text{ GHz}$ . These characteristics permit embedded ultra-low-voltage analog circuits and RF front-end circuits in combination with embedded DRAM cores for ultra-low-power, low-cost SOC.

**Key words:** dynamic-threshold DTMOS device, source/ drain, embedded DRAM technology

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## 0 Introduction

SOI CMOS solves several difficult SOC process integration problems, including well design, latch-up, digital-to-analog crosstalk, and improved DRAM retention. However, the typical partially-depleted SOI device must overcome non-linearity (kink), excess  $1/f$  noise, and reduced output resistance, due to the floating-body effects. The Dynamic Threshold (DTMOS) mode of SOI device operation has been shown to be superior to both body-tied (GB) and floating body (FB) modes for ultra-low-voltage, mixed-signal circuits<sup>[1-6]</sup>.

## 1 Process/ Device Description

The devices used in this work were processed in a 0.15  $\mu\text{m}$  CMOS DRAM stacked-capacitor process on low-dose SIMOX substrates (Table 1). This process includes a nitrided 4 nm gate oxide and WSi<sub>2</sub> poly gates, without silicided source/drains. Shallow S/D extensions, retrograde body, and halo implants were used to improve short-channel behavior. The interdigitated DTMOS transistor layout and cross-section are shown in Fig. 1. The gate and body stripes are locally interconnected to p<sup>+</sup> contacts at each end. The energy and dose of the “deep” S/D arsenic implants were varied in order to create various depths of S/D junction down to the buried oxide. Shallower S/D junctions ( $1\text{E}15$ , 10keV) allowed a lower resistance, wide path for the body current to flow under the device to the p<sup>+</sup> contacts at the ends, thus enhancing the dynamic body effect.

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**Biography:** Burke F. Jamaican, born in 1981, Master graduate at department of Electrical & Computer Engineering, Boise State University; his research interest includes IC design, device modeling and Characterization.

2 Results & Discussion

Table 2 summarizes the various electrical results of the S/D implant splits. Fig. 2 shows the DTMOS device, with 3X higher current drive than either the body-tied or floating-body devices. The threshold voltage is not yet optimized, and should be reduced by 0.3 V. Therefore,  $V_g = 1.3\text{ V}$ ,  $V_d = 1.0\text{ V}$  is used to define  $I_{on} = 656\text{ }\mu\text{A}/\mu\text{m}$ . Fig. 3 shows the subthreshold and transconductance curves. The  $I_{off} = 3\text{ pA}/\mu\text{m}$  will increase to about  $0.3\text{ }\mu\text{A}/\mu\text{m}$  after  $V_t$  optimization. A nearly ideal subthreshold swing of  $64\text{ mV}/\text{decade}$  and an impressive  $g_{msat} = 1\text{ }690\text{ }\mu\text{S}/\mu\text{m}$  are achieved.

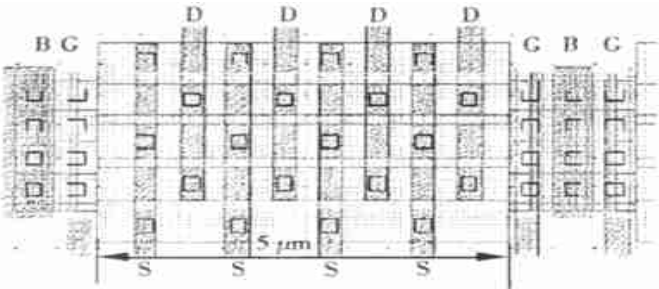


Fig. 1(a) Layout of the interdigitated DTMOS transistor, with four  $5\text{ }\mu\text{m}$  gate fingers and gate-to-body metal connections at both sides of the device. This  $W = 20\text{ }\mu\text{m}$  block is replicated 4 times to build a  $W = 80\text{ }\mu\text{m}$  RF transistor.

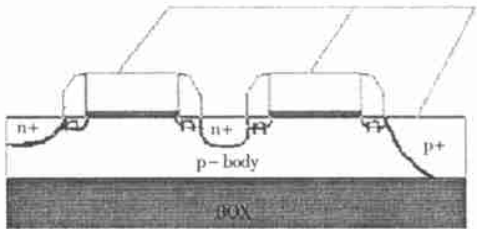


Fig. 1(b) Crossection sketch of the shallow S/D DTMOS device, showing the body contact on the right

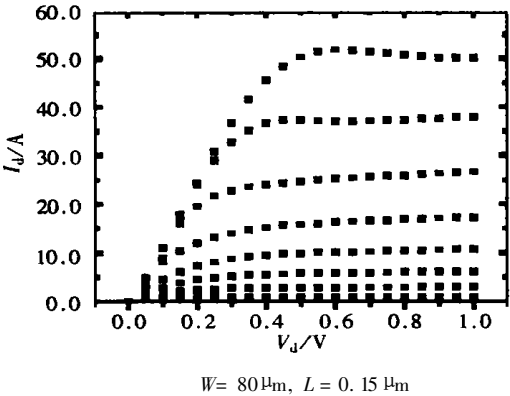


Fig. 2 DTMOS  $I_d$ - $V_d$  characteristic of the shallow S/D split.

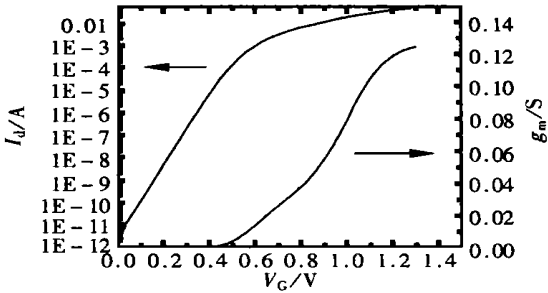


Fig. 3 DTMOS subthreshold &  $g_m$  characteristics

Fig. 4 show DIBL and Body Effect as a function of channel length down to  $L = 0.15\text{ }\mu\text{m}$ , for the DTMOS with the shallowest S/D split. These parameters vary with channel length in the same manner as conventional SOI MOSFETs. Fig. 5 shows the body effect and DIBL as a function of the S/D splits. The body effect is defined as the

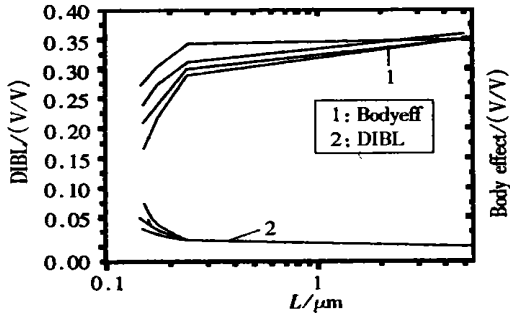


Fig. 4 DIBL and Body Effect vs. Channel Length

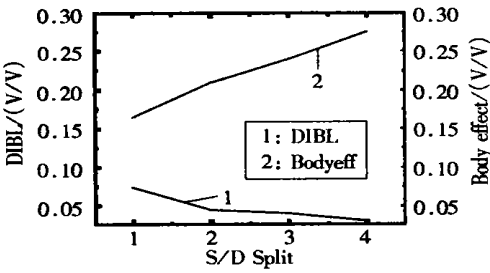


Fig. 5 DIBL and Body Effect vs. S/D splits

threshold voltage shift as the body bias is dynamically shifted by 1 V. DIBL is defined as the drain-induced threshold voltage shift for 1 V of drain bias. Fig. 6 shows the  $g_{\text{msat}}$  and  $I_{\text{on}}$  of the 0.15  $\mu\text{m}$  device as a function of the S/D splits. As both the S/D implant energy and dose are reduced, the drain junction becomes shallower, DIBL is reduced, while dynamic body effect is enhanced. This enhancement is due to a lower resistance path under the S/D to the p+ body contact, and leads to higher  $I_{\text{on}}$  and higher  $g_{\text{msat}}$ .

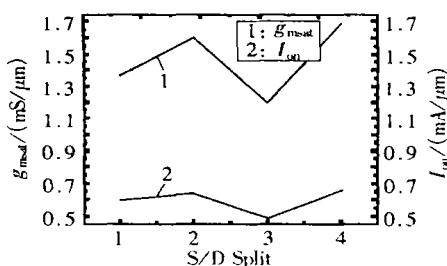


Fig 6  $g_{\text{msat}}$  and  $I_{\text{on}}$  vs. S/D splits

### 3 Acknowledgment

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## 基于 0.15 微米 SOI 嵌入式 DRAM 技术的动态钳制电位 DTMOS 器件源极与漏极的优化设计

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[ 摘要 ] 描述了用以进行  $n$ -沟道动态电位 DTMOS 半导体器件源极/漏极载流子注入优化设计的实验结果, 该器件制造采用了低成本 0.15 微米 SOI 和 SOC (system-on-chip, 系统集成芯片) 技术, 同时也包含了高密度嵌入式 DRAM 技术. 实验结果表明, 本器件可用来作为嵌入式超低压模拟电路和射频前端电路的混合电路芯片, 并与嵌入式 DRAM 核心技术一起, 作为超低压、低成本 SOC (系统集成芯片) 使用.

[ 关键词 ] 动态钳制电位 DTMOS 器件, 嵌入式 DRAM 技术, 系统集成芯片

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